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(54) Abstract Title
Data input-output circuits that selectively invert bits to save power

(57) A plurality of bits (RDAT) is output if more of the plurality of bits are of a first logical value than a second logical value, and the plurality of bits inverted is output if more of the plurality of bits are of the second logical value than the first logical value. An indicator (XCON) also is provided as to whether the plurality of bits or the plurality of bits inverted are output. Thus, for example, if more of the bits are of the logical value that causes high current consumption, the output bits are inverted so that the bits can be output with reduced current consumption. Upon receipt, the plurality of bits and the indicator are received. The plurality of bits is retained if the indicator is of a first value and the plurality of bits is inverted if the indicator is of a second value. Thus, the power consumption of the data input-output circuits may be reduced. The technique may be applied to memories with open-drain outputs.

FIG. 1

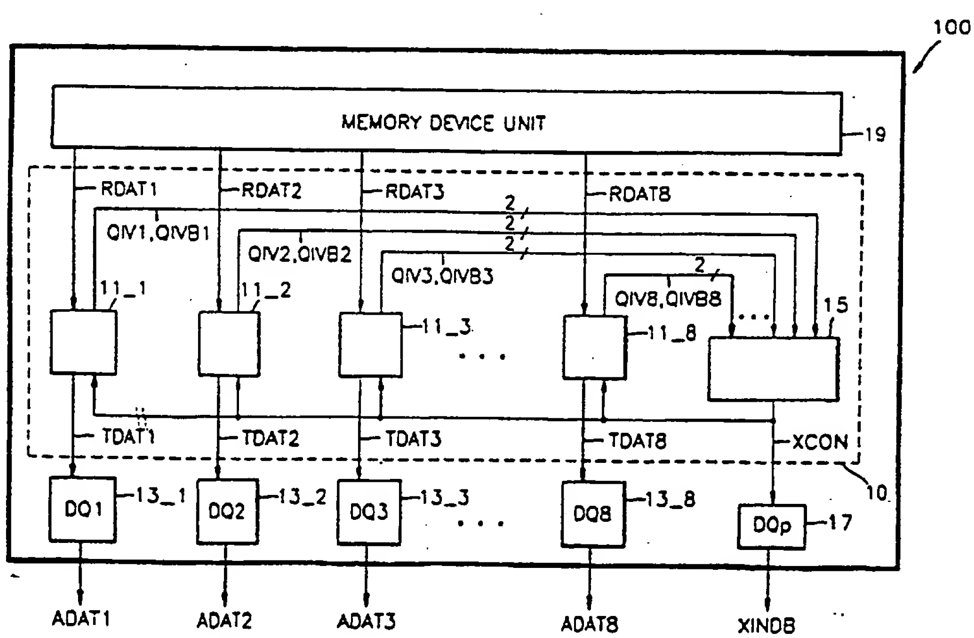

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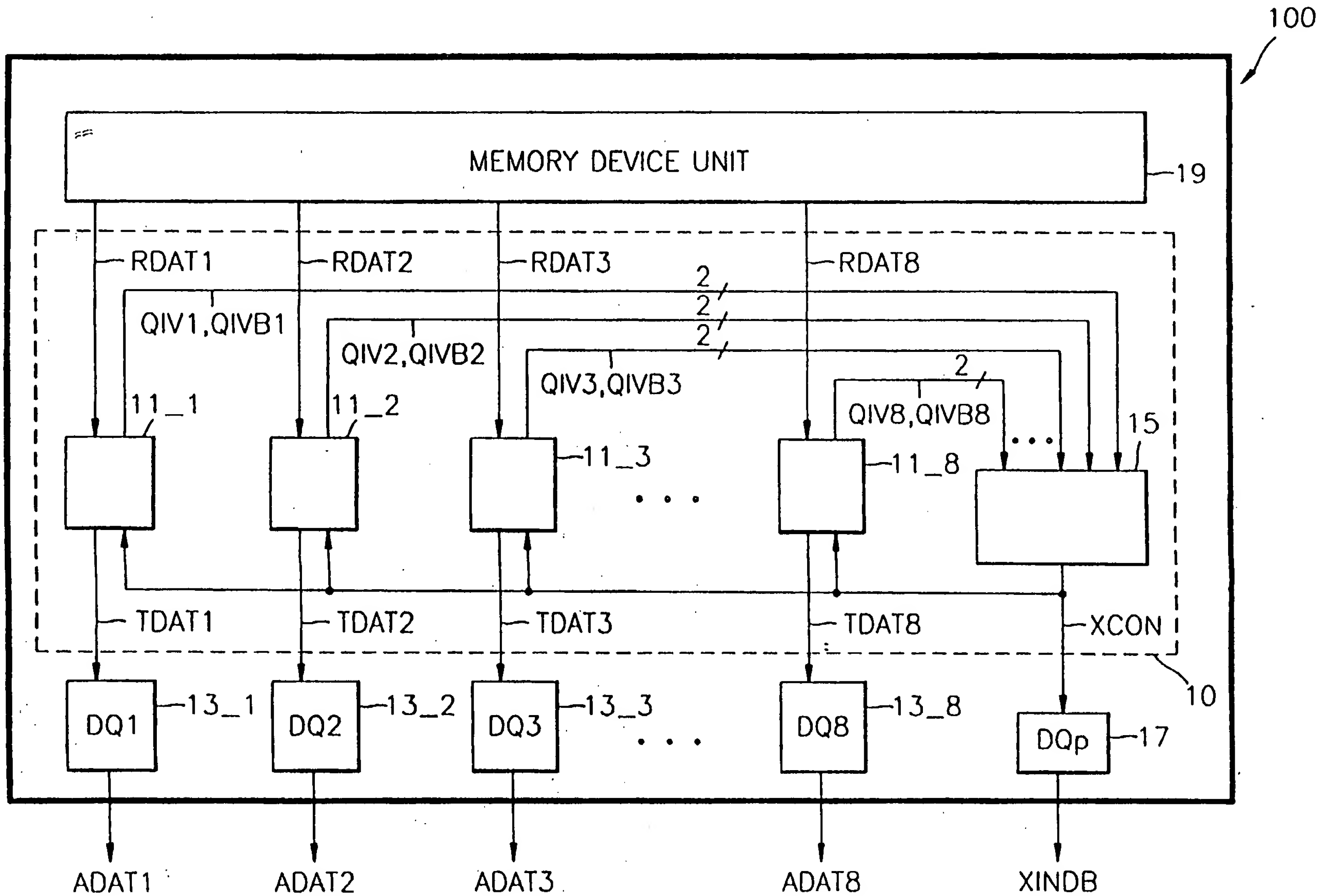
FIG. 1



100
MEMORY DEVICE UNIT
19
RDAT1
RDAT2
RDAT3
RDAT8
QIV1,QIVB1
QIV2,QIVB2
QIV3,QIVB3
QIV8,QIVB8
2
11_1
11_2
11_3
11_8
15
TDAT1
TDAT2
TDAT3
TDAT8
XCON
10
DQ1
DQ2
DQ3
DQ8
DQp
13_1
13_2
13_3
13_8
17
ADAT1
ADAT2
ADAT3
ADAT8
XINDB

FIG. 2

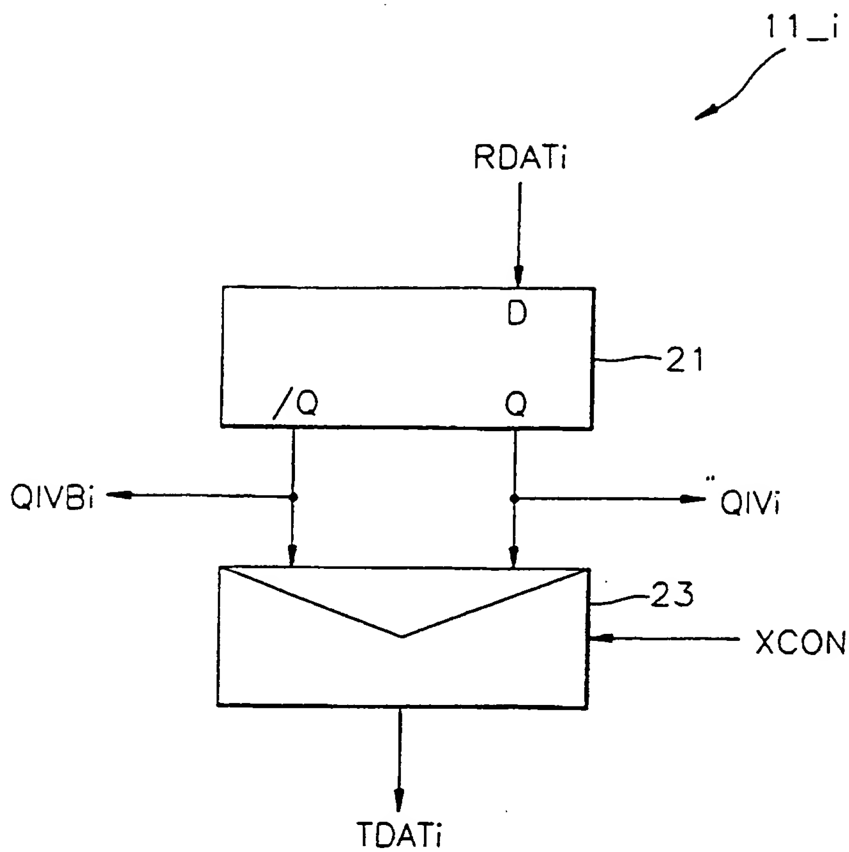


FIG. 3

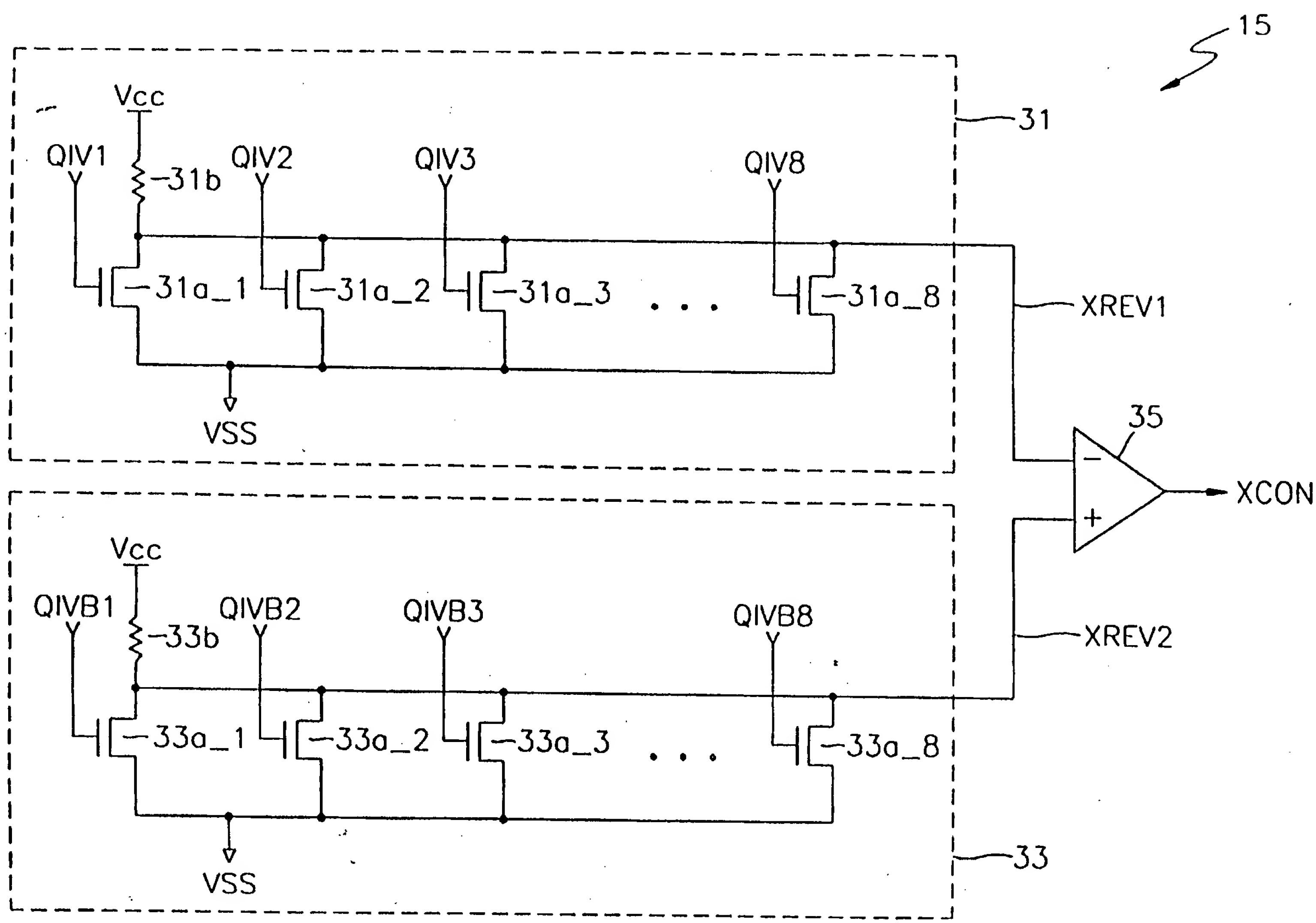

15
31
Vcc
QIV1
31b
QIV2
QIV3
QIV8
31a_1
31a_2
31a_3
31a_8
VSS
XREV1
35
XCON
Vcc
QIVB1
33b
QIVB2
QIVB3
QIVB8
33a_1
33a_2
33a_3
33a_8
VSS
XREV2
33

FIG. 4

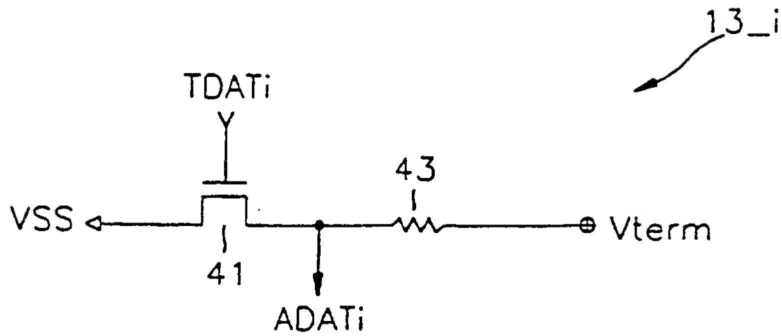

13_i
TDATi
43
VSS
Vterm
41
ADATi

FIG. 5

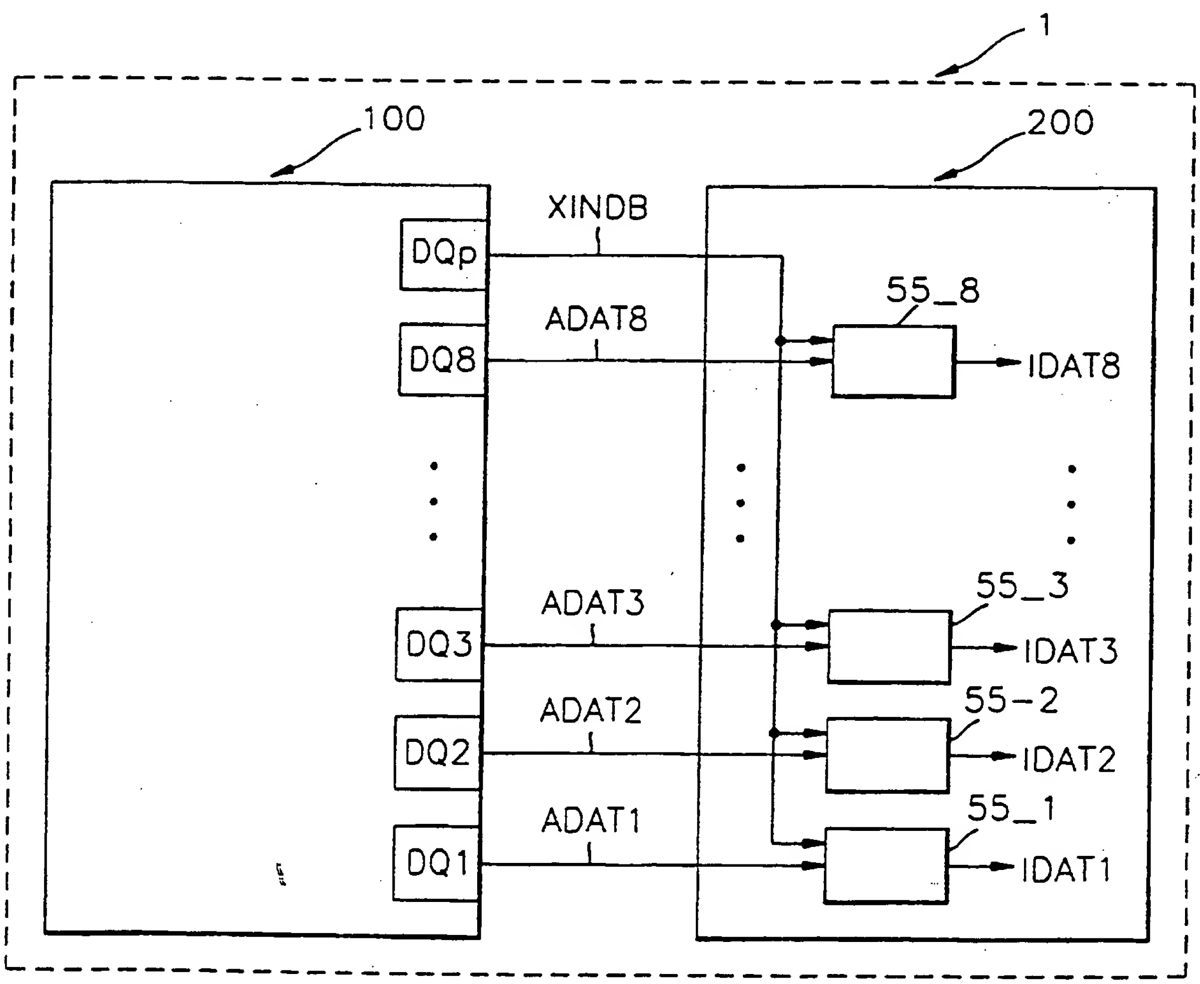
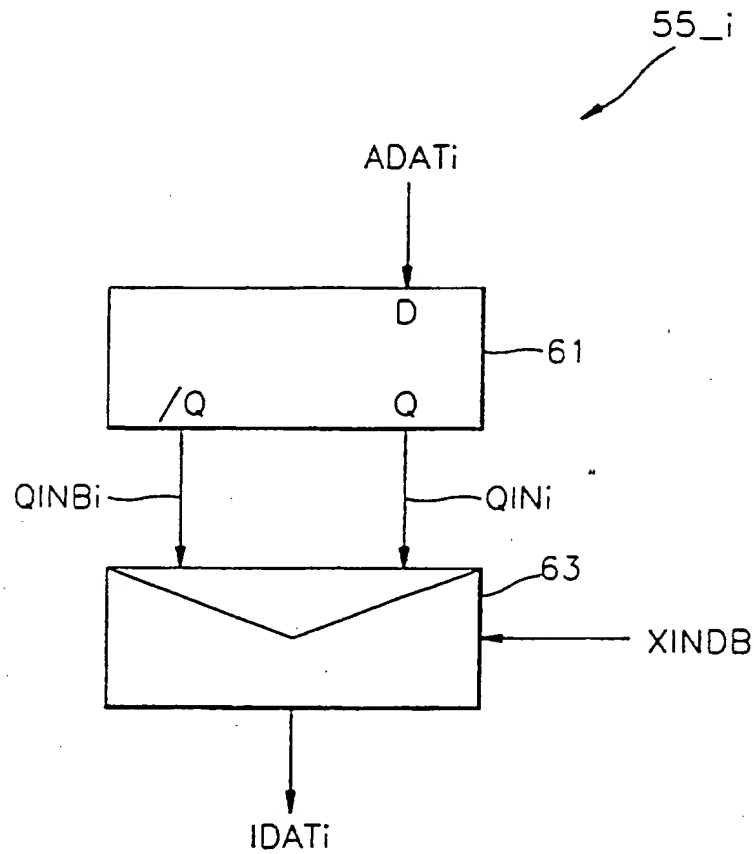

1
100
200
XINDB
DQp
55_8
ADAT8
DQ8
IDAT8
55_3
ADAT3
DQ3
IDAT3
55-2
ADAT2
DQ2
IDAT2
55_1
ADAT1
DQ1
IDAT1

FIG. 6



DATA INPUT-OUTPUT CIRCUITS AND METHODS THAT SELECTIVELY INVERT BITS

The present invention relates to integrated circuit devices and more particularly to data input-output circuits and methods for integrated circuit devices.

Integrated circuit devices, such as memory devices, are widely used in commercial and consumer applications. As integrated circuit devices continue to advance, high speed and high integration are generally desired. For such high-speed operation, the integrated circuit device may have an output unit with an open-drain structure.

An output unit with the open-drain structure has an output transistor where the drain port is floating. Either an NMOS or PMOS transistor can be used as the output transistor. When an NMOS transistor is used, the source port is connected to ground voltage (VSS) and the gate port receives real data to be output. In the open drain structure, the drain port of the output transistor is connected to a terminal voltage (Vterm) via a resistor. It will be understood that although an open-drain structure having an NMOS-type output transistor is described herein, PMOS devices also may be used.

Thus, when the real data is "0", the output transistor is turned off. The voltage level of the output signal at the drain port of the output transistor becomes the terminal voltage (Vterm). When the real data is "1", the output transistor is turned on. Thus, the voltage level of the output signal at the drain port of the output transistor is a value obtained by subtracting the voltage drop value across the resistor from the terminal voltage (Vterm). Thus, the output data of the open-drain output unit is

defined only as logic "1" which is a state of consuming current, or as logic "0" which is a state of non-consuming current.

The open-drain output unit has a predetermined swing width to produce the data output of "1" or "0". Thus, a predetermined positive current flows through the resistor, so that when the output data is "1", a great amount of current may be consumed.

For example, when the resistance value of the resistor is 20Ω, approximately 50mA of current flows from the terminal voltage (Vterm) to the ground voltage (VSS) to produce a swing width of about 1V. Thus, when 8 bits of output data having a data value of "1" are output, the open-drain output unit consumes a current of about 400mA(=50mA per bit). Unfortunately, such an increase in the amount of consumed current may decrease the efficiency and/or may shorten the life of the integrated circuit device.

According to a first aspect of the present invention, there is provided an output circuit for simultaneously outputting a plurality of data values **A** causing a current consumption of **a**, or **B** causing a current consumption of **b** which is more than the amount **a**. A plurality of data output units detect a plurality of real data values and generate temporary data corresponding to the respective real data in response to a control signal. A control unit generates the control signal which is activated according to the magnitude relation between the number of real data values A and the number of real data values **B**. The temporary data is the inverted real data when the number of real data values A is less than the number of real data values **B**, and the

non-inverted real data when the number of real data values A is greater than the number of real data values B.

The method of the invention outputs a plurality of bits if more of the plurality of bits are of a first logical value than a second logical value, and outputs the plurality of bits inverted if more of the plurality of bits are of the second logical value than the first logical value. This data input-output circuit can reduce power consumption compared to conventional input-output circuits. Thus, for example, if more of the bits are of the logical value that causes high current consumption, the output bits are inverted so that the bits can be output with reduced current consumption.

An indicator also preferably is provided as to whether the plurality of bits or the plurality of bits inverted are output. Upon receipt, the plurality of bits and the indicator are received. The plurality of bits is retained if the indicator is of a first value and the plurality of bits is inverted if the indicator is of a second value. Thus, the power consumption of the data input-output circuits may be reduced.

Preferably, the control unit includes a non-inversion detecting unit that detects the non-inverted data values of the real data and that generates a non-inversion detecting signal driven by the non-inverted data having the data values of B. An inversion detecting unit detects the inverted data values of the real data and generates an inversion detecting signal driven by the inverted data having the data values of A. A comparator compares the voltage level of the non-inversion detecting signal to the voltage level of the inversion detecting signal, and generates the control signal.

According to a second aspect of the present invention, there is provided an input-output system for simultaneously inputting and outputting a plurality of real data having data values of A causing a current consumption of **a**, or **B** causing a current consumption of **b** which is more than the amount **a**. The input-output system includes an output device that detects the data values of the real data and provides transmission data corresponding to the real data, and an indication signal (indicator) to indicate the relationship between the real data and the transmission data. An input device receives the transmission data and the indication signal and provides input data, whose relationship with the transmission data is determined by the indication signal, to an internal circuit. The transmission data is the inverted real data when the number of real data values having the data value of **A** is less than the number of real data values having the data value of **B**, and the non-inverted real data when the number of real data values having the data value of **A** is greater than the number of real data values having the data value of **B**. The input data has the same data value as the real data.

According to a third aspect of the present invention, there is provided an output device for simultaneously outputting a plurality of data. The output device includes a data storage unit that stores predetermined real data and provides a plurality of real data in an output mode. An output circuit receives the real data and generates temporary data according to the data values of the real data. The temporary data is the inverted real data when the number of real data values having a data value of **A** causing a current consumption of **a** is less than the number of real data values having a data value of **B** causing a current consumption of **b** that is more than the current amount **a**, and the non-inverted real data when the number of real data values having the data value of A is greater than the number of real data values having the data

value of B.

According to a fourth aspect of the present invention, there is provided a method of simultaneously outputting a plurality of data having a data value of **A** consuming a current amount of **a**, or **B** consuming a current amount of **b** which is more than the amount of a. This method comprises the steps of sensing the data values of a plurality of real data; comparing the number (m) of real data having the data value of **A** to the number (n) of real data having the data value of **B**; generating temporary data by inverting the real data when the number (m) is greater than the number (n), and by non-inverting the real data when the number (m) is less than the number (n); and generating an indication signal for indicating the correlation between the temporary data and the real data.

This method can reduce power consumption.

According to a fifth aspect of the present invention, there is provided a data input and output method having an input and output system having an input/output device for simultaneously inputting/outputting a plurality of data having a data value of **A** consuming a current amount of **a**, or **B** consuming a current amount of **b** which is more than the amount of **a**. This method preferably comprises the steps of detecting the data values of a plurality of real data; comparing the number (m) of real data having the data value of A to the number (n) of real data having the data value of **B**; generating temporary data by inverting the real data when the number (m) is less than the number (n), and by non-inverting the real data when the number (m) is greater than or equal to the number (n); generating a control signal for indicating the

correlation between the temporary data and the real data; and generating predetermined input data whose correlation with the temporary data is determined in response to the control signal. The input data has the same data value as the real data.

According to the present invention, when the number of data values causing large consumption of current is more than the number of data values causing a small consumption of current, the values of output data are inverted and output. The amount of current consumed therefore may be reduced. The reduction of the amount of current consumed can provide an increase in the efficiency and/or the life of an integrated circuit using the present invention.

Examples of the present invention will now be described in detail with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram illustrating an integrated circuit including a low current operation output circuit according to an embodiment of the present invention;

FIG. 2 is a block diagram illustrating a data output unit of FIG. 1;

FIG. 3 is a circuit diagram illustrating a control unit of FIG. 1;

FIG. 4 is a circuit diagram illustrating an output pad unit of FIG. 1;

FIG. 5 is a block diagram illustrating an embodiment of a low current operation input-output system using a low current operation output circuit according to the present invention; and,

FIG. 6 is a block diagram illustrating the data input circuit of FIG. 5.

Like numbers refer to like elements throughout. Moreover, each embodiment

described and illustrated herein includes its complementary conductive type embodiment as well.

FIG. 1 shows an output device **100** having a low current operation output circuit **10** according to an embodiment of the present invention. The output device **100** preferably corresponds to a portion of, or a complete, integrated circuit. The low current operation output circuit **10** simultaneously outputs a plurality of bits each having a logic value of either "0" or "1". For the sake of convenience, in this specification, a low current operation output circuit **10** that simultaneously outputs 8 bits of data is described as an example.

Data output units **11_i** (where i=1 through 8) receive real data **RDATi** (where i=1 through 8) output from a memory device unit **19**, and generate corresponding temporary data **TDATi** (where i=1 through 8). When the number of "1" data value is greater than the number of "0" data values in the real data (RDATi), RDATi is inverted to produce temporary data **TDATi** corresponding respectively to **RDATi**. When the number of "1" data values is less than the number of "0" data values in the real data (RDATi), TDATi is non-inverted data of **RDATi**.

A control unit **15** detects the magnitude relationship between the number of real data values **RDATi** having the data value of "1" and the number of real data values **RDATi** having the data value of "0", and generates a control signal **XCON**. The control signal **XCON** controls the data output units (**11_i**) and determines the temporary data **TDATi** and the real data **RDATi**.

Output pad units **13_i** (where i=1 through 8) generate transmission data **ADATi** (where i=1 through 8) in response to the temporary data **TDATi**. The output pad units (13_i) have an open-drain structure. An output transistor of each of the output pad units (13_i) is assumed to be an NMOS transistor. Thus, the output pad units (13_i) consume much current when a data value of "1" is input, and consume very little current when a data value of "0" is input. An auxiliary output pad unit **17** receives the control signal **XCON** and externally provides an indication signal, also referred to as an indicator, **XINDB**.

FIG. 2 shows the data output unit 11_i of FIG. 1. To be more specific, the data output unit **11_i** includes a dual output unit **21** and a selector **23**.

The dual output unit **21** receives the real data **RDATi** and generates inverted data **QIVBi** (where i=1 through 8) and non-inverted data **QIVi** (where i=1 through 8) from the real data **RDATi**. Preferably, the dual output unit **21** is a D flip-flop.

The selector **23** receives the inverted data **QIVBi** (where i=1 through 8) and non-inverted data **QIVi** (where i=1 through 8) of the real data **RDATi**, and generates the temporary data **TDATi** in response to the control signal **XCON**. That is, when the control signal **XCON** is activated, the temporary data **TDATi** is the inverted data **QIVBi** of the real data **RDATi**. When the control signal **XCON** is deactivated, the temporary data **TDATi** is the non-inverted data **QIVi** of the real data **RDATi**. Preferably, the selector **23** is a 2:1 multiplexer.

FIG. 3 shows the control unit **15** of FIG. 1. Referring to FIG. 3, the control unit **15**

includes a non- inversion detecting unit **31**, an inversion detecting unit **33**, and a comparator **35**.

The non-inversion detecting unit **31** detects the value of the non-inverted data **QIVi** of the real data **RDATi**, and generates a non-inversion detecting signal **XREV1** whose voltage level drops according to the number of non-inverted data values **QIVi** having a data value of "1".

To be more specific, the non-inversion detecting unit **31** includes first NMOS transistors **31a_i** (where, i=1 through 8) and a first resistor **31b**. Each of the first group of NMOS transistors **31a_i** (where, i=1 through 8) have a source port connected to the ground voltage **VSS**, and gate ports to which the non-inverted data values **QIVi** of the corresponding real data **RDATi** are applied. The first resistor **31b** connects the drain port of the first NMOS transistor **31a_i** to a power supply voltage **VCC**. The drain port of the first NMOS transistor **31a_i** outputs the non-inversion detecting signal **XREV1**.

Accordingly, the voltage level of the non-inversion detecting signal **XREV1** lowers in response to an increase in the number of non-inverted data values **QIVi** having a data value of "1". That is, as the number of real data values **RDATi** having a value of "1" increases, the voltage level decreases.

The inversion detecting unit **33** detects the value of the inverted data **QIVBi** of the real data **RDATi**. The inversion detecting unit **33** generates an inversion detecting signal **XREV2** whose voltage level decreases according to the number of inverted

data values QIVBi having a data value of "1".

To be more specific, the inversion detecting unit **33** includes second NMOS transistors **33a_i** (where i=1 through 8) and a second resistor **33b**. The second NMOS transistors **33a_i** (where i=1 through 8) have a source port connected to the ground voltage **VSS**, and gate ports to which the inverted data **QIVBi** of the real data **RDATi** is applied. The second resistor **33b** connects the drain port of the second NMOS transistor **33a_i** to the power supply voltage **VCC**. The drain port of the second NMOS transistor outputs the inversion detecting signal **XREV2**.

Accordingly, the voltage level of the inversion detecting signal **XREV2** decreases in response to an increase in the number of inverted data values **QIVBi** having a data value of "1". That is, as the number of real data values **RDATi** having a value of "0" increases, the voltage level decreases.

The comparator **35** compares the voltage level of the non-inversion detecting signal **XREV1** to the voltage level of the inversion detecting signal **XREV2**, and generates the control signal **XCON**. To be more specific, the non-inversion detecting signal **XREV1** is applied to an inversion input port (-) of the comparator **35**, and the inversion detecting signal **XREV2** is applied to a non-inversion input port (+) of the comparator **35**.

The comparator **35** is designed to be deactivated when the voltages of the inversion and non- inversion input ports (-) and (+) are the same. Thus, when the voltage level of the non-inversion detecting signal **XREV1** is lower than that of the inversion

detecting signal **XREV2**, the control signal **XCON** is activated. That is, when the number of real data values **RDATi** having a data value of "0" is greater than the number of real data values **RDATi** having a data value of "1", the control signal **XCON** is activated to be "high". However, when the voltage level of the non-inversion detecting signal **XREV1** is higher than or equal to that of the inversion detecting signal **XREV2**, the control signal **XCON** is deactivated. That is, when the number of real data **RDATi** having a data value of "0" is less than the number of real data **RDATi** having a data value of "1", the control signal **XCON** is deactivated to be "low". The control signal **XCON** also preferably is deactivated to "low" when the number of real data **RDATi** having a data value of "0" is equal to the number of real data **RDATi** having a data value of "1."

FIG. 4 shows the output pad unit **13_i** of FIG. 1. Referring to FIG. 4, the output pad unit **13_i** includes an output transistor **41** and a resistor **43** also referred to as an end resistor. The output transistor **41** is an NMOS transistor having a source port to which the ground voltage **VSS** is connected, and a gate port to which temporary data **TDATi** is applied. The end resistor **43** connects the terminal voltage **Vterm** to the drain port of the output transistor **41**. The drain port of the output transistor **41** outputs the transmission data **ADATi**.

Thus, when the temporary data **TDATi** is "1", the output pad unit **13_i** consumes a great amount (about 50mA) of current. However, when the temporary data **TDATi** is "0", the output pad unit **13_i** consumes little or no current.

Tables 1 and 2 show the data values of the temporary data **TDATi** and control signal

XCON when the number of real data **RDATi** having a data value of "1" is greater than that of real data **RDATi** having a data value of "0".

Table 1

i	1	2	3	4	5	6	7	8	XCON
RDATi	1	1	1	1	1	1	1	1	X
TDATi	0	0	0	0	0	0	0	0	1

Table 1 shows the case that all the data values of the real data **RDATi** are "1". Here, the data value of the control signal **XCON** is "1", so the temporary data **TDATi** is the inverted data of the real data **RDATi**. X indicates that no control signal **XCON** exists when the low current operation output circuit of the present invention is not used.

If the real data **RDATi** is non-inverted and output, the amount of consumed current is about 400mA(=50mA per bit) which is consumed by the output pad units **13_i**. However, when the temporary data **TDATi** obtained by inverting the real data **RDATi** is output, the amount of consumed current is only about 50mA which is consumed by the output of the control signal **XCON**. Thus, about 350mA of current consumption can be saved by the low current operation output circuit **10** of the present invention.

Table 2

i	1	2	3	4	5	6	7	8	XCON
RDATi	1	1	0	0	0	1	1	1	X
TDATi	0	0	1	1	1	0	0	0	1

Table 2 shows the case that there are 5 real data **RDATi** having the data value of "1" and 3 real data **RDATi** having the data value of "0". Here, the data value of the control signal **XCON** is "1", so the temporary data **TDATi** is the inverted data of the real data **RDATi**.

If the real data **RDATi** is non-inverted and output, the amount of consumed current is about 250mA(=50mA per bit) which is consumed by five of the output pad units **13_i**. However, when the temporary data **TDATi** is output by inverting the real data **RDATi**, the amount of consumed current is about 150mA(=50mA per bit) which is consumed by the three output pad units **13_i** and about 50mA which is consumed by the output of the control signal **XCON**. Thus, the total amount of consumed current is about 200mA, so about 50mA of current consumption may be saved by the low current operation output circuit **10** of the present invention.

Table 3 shows the data values of the temporary data **TDATi** and control signal **XCON** when the number of real data **RDATi** having a data value of "1" is equal to that of real data **RDATi** having a data value of "0".

Table 3

i	1	2	3	4	5	6	7	8	
RDATi	1	0	0	1	0	0	1	1	X
TDATi	1	0	0	1	0	0	1	1	0

Table 3 shows the case that there are 4 real data **RDATi** having the data value of "1" and 4 real data **RDATi** having the data value of "0". Here, the data value of the control signal **XCON** preferably is "0", so the temporary data **TDATi** is the non-

inverted data of the real data **RDATi**.

If the real data **RDATi** is non-inverted and output, the amount of consumed current is about 200mA(=50mA per bit) which is consumed by the four output pad units **13_i**. However, when the temporary data **TDATi** is output by inverting the real data **RDATi**, the amount of consumed current is about 200mA(=50mA per bit) which is consumed by the four output pad units **13_i** and about 50mA which is consumed by the output of the control signal **XCON**. Thus, the total amount of consumed current is about 250mA, so about 50mA of current consumption is added when the temporary data **TDATi** is output by inverting the real data **RDATi**. Therefore, when the number of real data **RDATi** having the data value of "1" is equal to that of real data **RDATi** having the data value of "0", the temporary data **TDATi** preferably is the non-inverted data of the real data **RDATi**. Thus, the current consumption can be reduced by about 25% by the low current operation output circuit **10** of the present invention.

FIG. 5 shows an example of a low current operation system according to the present invention. Referring to FIG. 5, a low current operation system **1** includes an output device **100** and an input device **200**. It will be understood that devices **100** and **200** may be separate integrated circuits or may be integrated into a single integrated circuit.

The output device **100** is as shown in FIG. 1. That is, the output device **100** inverts the real data **RDATi** and outputs the transmission data **ADATi** when the number of real data **RDATi** (not shown in FIG. 5) having the data value of "1" is greater than

the number of real data **RDATi** having the data value of "0". The output device **100** does not invert the real data **RDATi** and outputs the transmission data **ADATi** when the number of real data **RDATi** having the data value of "1" is less than or equal to the number of real data **RDATi** having the data value of "0". A detailed embodiment of the output device **100** is as shown in FIG. 1 and need not be described in detail again.

The input device **200** will now be described in detail. The input device **200** receives the transmission data **ADATi** and the indication signal **XINDB** and generates input data **IDATi** (where i=1-8). The indication signal **XINDB** has an inverted state of the control signal **XCON** (refer to FIG. 1). That is, the input data **IDATi** is the inverted data of the transmission data **ADATi** when the indication signal **XINDB** is activated. The input data **IDATi** is the non-inverted data of the transmission data **ADATi** when the indication signal **XINDB** is deactivated. Accordingly, the input data values **IDATi** have the same data values as the real data **RDATi**.

The input device **200** includes a plurality of data input circuits **55_i** (where i=1-8). The data input circuits **55_i** receive the transmission data **ADATi** corresponding to the respective data input circuits **55_i** and generate the input data **IDATi** under the control of the indication signal **XINDB**.

FIG. 6 shows a data input circuit **55_i** of FIG. 5. Referring to FIG. 6, the data input circuit **55_i** includes a dual output unit **61** and a selector **63**. The dual output unit **61** receives the transmission data **ADATi** and generates the inverted data **QINBi** and non-inverted data **QINi** of the transmission data **ADATi**.

The selector 63 receives the inverted data **QINBi** and non-inverted data **QINi** of the transmission data **ADATi**, and generates the input data **IDATi** in response to the indication signal **XINDB**. That is, the input data **IDATi** when the indication signal **XINDB** is activated has the same data value as the inverted data **QINBi** of the transmission data **ADATi**. The input data **IDATi** when the indication signal **XINDB** is deactivated has the same data value as the non-inverted data **QINi** of the transmission data **ADATi**. Thus, the input data **IDATi** has the same data value as the real data **RDATi**.

The present invention was described with reference to the embodiment shown in the drawings, but the embodiment is just an example. It will be understood by those skilled in the art that various modifications and other embodiments may be effected. For example, the output transistor of the output pad unit **13_i** is described as an NMOS transistor, but can be a PMOS transistor. For a PMOS transistor, the source port of the output transistor is connected to the power supply voltage, and the drain port thereof is connected to the terminal voltage via the end resistor. When the output transistor is the PMOS transistor, much current is consumed when a data value of "0" is output. Thus, in this case, it is apparent to those skilled in the art that when the number of real data **RDATi** having a data value of "0" is greater than the number of real data **RDATi** having a data value of "1", the output transistor may be designed to be activated. Finally, it was described that the low current operation output device in the present specification simultaneously outputs 8 bits of data, but it is also apparent that the number of data output simultaneously can be increased or decreased.

In the drawings and specification, there have been disclosed typical preferred

embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

CLAIMS:

1. An output circuit for simultaneously outputting a plurality of data values **A** causing a current consumption of **a**, or **B** causing a current consumption of **b** which is more than the amount **a**, the circuit comprising:

a plurality of data output units that detect a plurality of real data values and that generate temporary data corresponding to the respective real data in response to a control signal; and,

a control unit that generates the control signal which is activated according to the magnitude relation between the number of real data values **A** and the number of real data values **B**;

wherein the temporary data is the inverted real data when the number of real data values **A** is less than the number of real data values **B**, and the non-inverted real data when the number of real data values **A** is greater than the number of real data values **B**.

2. The output circuit as claimed in Claim 1, wherein the control unit comprises:

a non-inversion detecting unit that detects the non-inverted data values of the real data and that generates a non-inversion detecting signal driven by the non-inverted data having the data values of **B**;

an inversion detecting unit that detects the inverted data values of the real data and that generates an inversion detecting signal driven by the inverted data having the data values of **A**; and,

a comparator that compares the voltage level of the non-inversion detecting signal to the voltage level of the inversion detecting signal, and that generates the control signal.

3. The output circuit as claimed in Claim 2, wherein the control signal is deactivated when the number of real data having the data values of A is equal to the number of real data having the data values of B.

4. The output circuit as claimed in Claim 3, wherein the non-inversion detecting unit comprises:

first NMOS transistors, the source ports of which are each connected to a ground voltage, and which are gated by the non-inverted data of the corresponding real data; and

first resistors that connect the drain ports of the first NMOS transistors to a power supply voltage, and,

wherein the inversion detecting unit comprises:

second NMOS transistors the source ports of which are each connected to the ground voltage and which are gated by the inverted data of the corresponding real data; and second resistors that connect the drain ports of the second NMOS transistors to the power supply voltage.

5. The output circuit as claimed in Claim 1, wherein each of the data output units comprises:

a dual output unit that receives the real data and that generates the inverted and non-inverted real data; and,

a selector that receives the inverted and non-inverted real data and that generates the temporary data.

6. The output circuit as claimed in Claim 5, wherein the dual output unit is a D-type

flip-flop.

7. The output circuit as claimed in Claim 5, wherein the selector outputs the inverted real data in response to activation of the control signal, and the non-inverted real data in response to deactivation of the control signal.

8. An input-output system for simultaneously inputting and outputting a plurality of real data having data values of A causing a current consumption of a, or B causing a current consumption of b which is more than the amount a,.the system comprising:

an output device that detects the data values of the real data and that provides transmission data corresponding to the real data, and an indication signal for indicating the relationship between the real data and the transmission data; and

an input device that receives the transmission data and the indication signal and that provides input data to an internal circuit, wherein the relationship of the input data to the transmission data is determined by the indication signal;

wherein the transmission data is the inverted real data when the number of real data values having the data value of A is less than the number of real data values having the data value of B, and the non-inverted real data when the number of real data values having the data value of A is greater than the number of real data values having the data value of B, and,

wherein the input data has the same data value as the real data.

9. The input-output system as claimed in Claim 8,. wherein the output device comprises:

a plurality of data output units that generate temporary data corresponding to the real

data;

a plurality of output pad units having an open-drain structure, that output the temporary data; and,

an auxiliary output pad unit that generates an indication signal to indicate the correlation between the temporary data and the real data;

wherein the temporary data is the inverted real data when the number of real data values having the data value of A is less than the number of real data values having the data value of B, and the non-inverted real data when the number of real data values having the data value of A is greater than the number of real data values having the data value of B.

10. The input-output system as claimed in Claim 9, wherein each of the data output units comprises:

a dual output unit that receives the real data and that generates the inverted and non-inverted real data; and,

a selector that receives the inverted and non-inverted data of the real data and that generates the temporary data.

11. The input-output system as claimed in Claim 10, wherein the dual output unit is a D- type flip-flop.

12. The input-output system as claimed in Claim 10, wherein the output device further comprises:

a control unit that generates a control signal which is activated when the number of real data values having the data value of A is less than the number of real data values

having the data value of **B**; and,

wherein the selector outputs the inverted real data in response to the activation of the control signal, and the non-inverted real data in response to the deactivation of the control signal.

13. The input-output system as claimed in Claim 8, wherein the input device comprises:

a plurality of data input circuits that receive the transmission data and that generate the input data under the control of the control signal.

14. An output device for simultaneously outputting a plurality of data, comprising:

a data storage unit that stores predetermined real data and provides a plurality of real data in an output mode; and,

an output circuit that receives the real data and that generates temporary data according to the data values of the real data;

wherein the temporary data is the inverted real data when the number of real data values having a data value of **A** causing a current consumption of **a** is less than the number of real data values having a data value of **B** causing a current consumption of **b** that is more than the current amount a, and the non-inverted real data when the number of real data values having the data value of **A** is greater than the number of real data values having the data value of **B**.

15. The output device as claimed in Claim 14, wherein the output circuit comprises:

a plurality of data output units that detect the real data and that generate temporary data corresponding to the real data;

a plurality of output pad units having an open-drain structure, that output the temporary data; and,

an auxiliary output pad unit that generates an indication signal to indicate the correlation between the temporary data and the real data.

16. The output device as claimed in Claim 15, wherein the output circuit further comprises:

a control unit that generates the control signal which is activated according to the magnitude relation between the number of real data values A and the number of real data values B.

17. The output device as claimed in Claim 15, wherein each of the data output units comprises:

a dual output unit that receives the real data and that generates the inverted and non-inverted real data; and

a selector that receives the inverted and non-inverted real data and that generates the temporary data.

18. The output device as claimed in Claim 17, wherein the dual output unit is a D-type flip-flop.

19. The output device as claimed in Claim 17, wherein the output circuit further comprises:

a control unit that generates a control signal which is activated when the number of real data values having the data value of A is less than the number of real data values

is deactivated.

23. A data input and output method for an input and output system having an input/output device for simultaneously inputting/outputting a plurality of data having a data value of A consuming a current amount of a, or B consuming a current amount of b which is more than the amount of a, the method comprising the steps of:
sensing the data values of a plurality of real data;
comparing the number (m) of real data having the data value of A to the number (n) of real data having the data value of B;
generating temporary data by inverting the real data when the number (m) is less than the number (n), and by non-inverting the real data when the number (m) is greater than the number (n);
generating a control signal to indicate the correlation between the temporary data and the real data; and
generating predetermined input data the correlation of which, with the temporary data, is determined in response to the control signal,
wherein the input data has the same data value as the real data.

24. The data input and output method as claimed in claim 23, wherein the control signal is activated when the number (m) is less than the number (n).

25. The data input and output method as claimed in claim 24, wherein the step of generating temporary data comprises the steps of:
receiving the real data and generating the inverted and non-inverted real data;
generating the inverted real data as the temporary data when the control signal is

activated; and

generating the non-inverted real data as the temporary data when the control signal is deactivated.

26. A data output system comprising:

means for providing a plurality of bits, each bit being of a first or a second logical value; and

means for outputting the plurality of bits if more of the plurality of bits are of the first logical value than the second logical value and for outputting the plurality of bits inverted if more of the plurality of bits are of the second logical value than the first logical value.

27. A data output system according to Claim 26 wherein the means for outputting further comprises means for indicating whether the plurality of bits or the plurality of bits inverted are output.

28. A data output system comprising:

a circuit that provides a plurality of bits, each bit being of a first or a second logical value; and

an output circuit that outputs the plurality of bits if more of the plurality of bits are of the first logical value than the second logical value and that outputs the plurality of bits inverted if more of the plurality of bits are of the second logical value than the first logical value.

29. A data output system according to Claim 28 wherein the output circuit also

indicates whether the plurality of bits or the plurality of bits inverted are output.

30. A data output method for a plurality of bits, each bit being of a first or second logical value, the data output method comprising the steps of:

outputting the plurality of bits if more of the plurality of bits are of the first logical value than the second logical value; and

outputting the plurality of bits inverted if more of the plurality of bits are of the second logical value than the first logical value.

31. A data output method according to Claim 30 further comprising the step of:

indicating whether the plurality of bits or the plurality of bits inverted are output.

32. A data receiving system comprising:

means for receiving a plurality of bits and an indicator, each bit being of a first or second logical value; and

means for retaining the plurality of bits if the indicator is of a first value and for inverting the plurality of bits if the indicator is of a second value.

33. A data receiving system according to Claim 32 wherein the indicator is of the first value to indicate that the plurality of bits were not inverted prior to receipt by the means for receiving, and is of the second value to indicate that the plurality of bits were inverted prior to receipt by the means for receiving.

34. A data receiving system comprising:

a receiver circuit that receives a plurality of bits and an indicator, each bit being of

a first or second logical value; and

a selective inverter circuit that retains the plurality of bits if the indicator is of a first value and that inverts the plurality of bits if the indicator is of a second value.

35. A data receiving system according to Claim 34 wherein the indicator is of the first value to indicate that the plurality of bits were not inverted prior to receipt by the receiver circuit, and is of the second value to indicate that the plurality of bits were inverted prior to receipt by the receiver circuit.

36. A data receiving method for a plurality of bits and an indicator, each bit being of a first or second logical value, the data receiving method comprising the steps of:

retaining the plurality of bits if the indicator is of a first value; and

inverting the plurality of bits if the indicator is of a second value.

37. A data receiving method according to Claim 36 wherein the indicator is of the first value to indicate that the plurality of bits were not inverted prior to receipt, and is of the second value to indicate that the plurality of bits were inverted prior to receipt.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H3P (PHFN,PHX) H4P (PDD,PDX)

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Other: Online: EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,Y	US5630106	Ricoh. See figures 1,4,5, and 7.	X: 32,34,36 Y: 5,7,10,12, 17,19, 22,25
X	US4667337	Westinghouse. See the abstract and figures.	32-37
X,Y	US4495626	IBM. See the abstract, figures 1 and 2b, and column 1 lines 18-21.	X:1,8,9, 13-16,20, 21,23,24, 26-37 Y: 5,7,10,12, 17,19, 22,25

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